ABSTRACT:

The method according to the present invention relates to the detection of fabrication defects in static CMOS circuits. An integrated circuit, for instance, having a gate (12, 13) additionally includes two sleep transistors (14, 15) and two pull transistors (16, 17) of regular threshold and low leakage. The sleep transistors are used to break up the gate into two parts (12; 13) for allowing a pair of response sequences. The two responses are either checked for consitency or compared against a predetermined expected response sequence. The usage of the pull transistors is as passive loads such as to enable pseudo NMOS and pseudo PMOS operation. One of the advantages of the method according to the invention, is that it is insensitive to MOSFET leakage currents.

Fig. 2